CLAIMS

What is claimed is:

1. A method comprising:

providing a semiconductor package having a first pad and a second pad;

depositing a first layer comprising a first metal on the first pad a using a first process; and

depositing a second layer comprising a second metal on the second pad and the first layer using a second process.

2. The method of claim 1, further comprising:

depositing a third layer over the first layer and the second pad with the first metal using a third process.

3. The method of claim 1, wherein the first metal comprises nickel, and the second metal comprises gold.

4. The method of claim 3, wherein using the first process comprises using an electroplating process, and wherein using the second process comprises using a direct immersion gold (DIG) process.

5. The claim of method 2, wherein using the third process comprises using an electroless plating process.

6. The method of claim 1, wherein the first pad comprises a power pad and a ground pad, and wherein the second pad comprises a signal pad.

7. The method of claim 4, further comprising:

forming a tie bar on the first pad to facilitate the electroplating process.

8. The method of claim 7, further comprising:

forming a plating bar surrounding the semiconductor package and coupled to the tie bar to direct current to the first pad.

9. The method of claim 1, further comprising:

placing an interconnect on the first pad and the second pad.

10. The method of claim 9, wherein the interconnect is chosen from the group consisting of a Ball Grid Array (BGA) interconnect, a Pin Grid Array (PGA) interconnect, and a Controlled Collapse Chip Connect (C4) interconnect.

11. The method of claim 2, further comprising:

placing a Land Grid Array (LGA) interconnect on the first and second pads.

12. An apparatus comprising:

a semiconductor package having a first pad and a second pad;

wherein the first pad has a first metal deposited thereon using a first process and a second metal deposited thereon using a second process; and wherein the second pad has the second metal deposited thereon using the second process.

13. The apparatus of claim 12, wherein the first metal is nickel and the second metal is gold.

14. The apparatus of claim 13, wherein the first process is electroplating and the second process is a direct immersion gold (DIG) deposition.

15. The apparatus of claim 12, wherein the first pad comprises a power and a ground pad, and wherein the second pad comprises a signal pad.

16. The apparatus of claim 12, further comprising:

a Ball Gird Array (BGA) interconnect coupled to the first and second pads.

17. The apparatus of claim 16, further comprising:

a printed circuit board (PCB) having a first pad and a second pad coupled to the BGA interconnect;

wherein the first pad has a first metal deposited thereon using a first process and a second metal deposited thereon using a second process; and

wherein the second pad has the second metal deposited thereon using the second process.

18. A method comprising:

providing a semiconductor package having a power pad and a signal pad;

attaching a tie bar to the power pad;

depositing a nickel layer on the power pad using an electroplating process by directing current through the tie bar; and

depositing a gold layer on the nickel layer and the signal pad and the nickel layer using a direct immersion gold (DIG) process.

19. The method of claim 18, further comprising:

depositing a second nickel layer on the signal pad and the nickel layer using an electroless deposition process before depositing the gold layer.

20. The method of claim 18, further comprising:

attaching the pads to a ball grid array (BGA) interconnect.

21. The method of claim 18, further comprising:

attaching the pads to a pin grid array interconnect.

22. The method of claim 18, wherein directing comprises attaching a plating bar to the tie bar, wherein the plating bar surrounds the package substrate, and electrifying the plating bar.